

Compal Confidential

NAV50/60 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

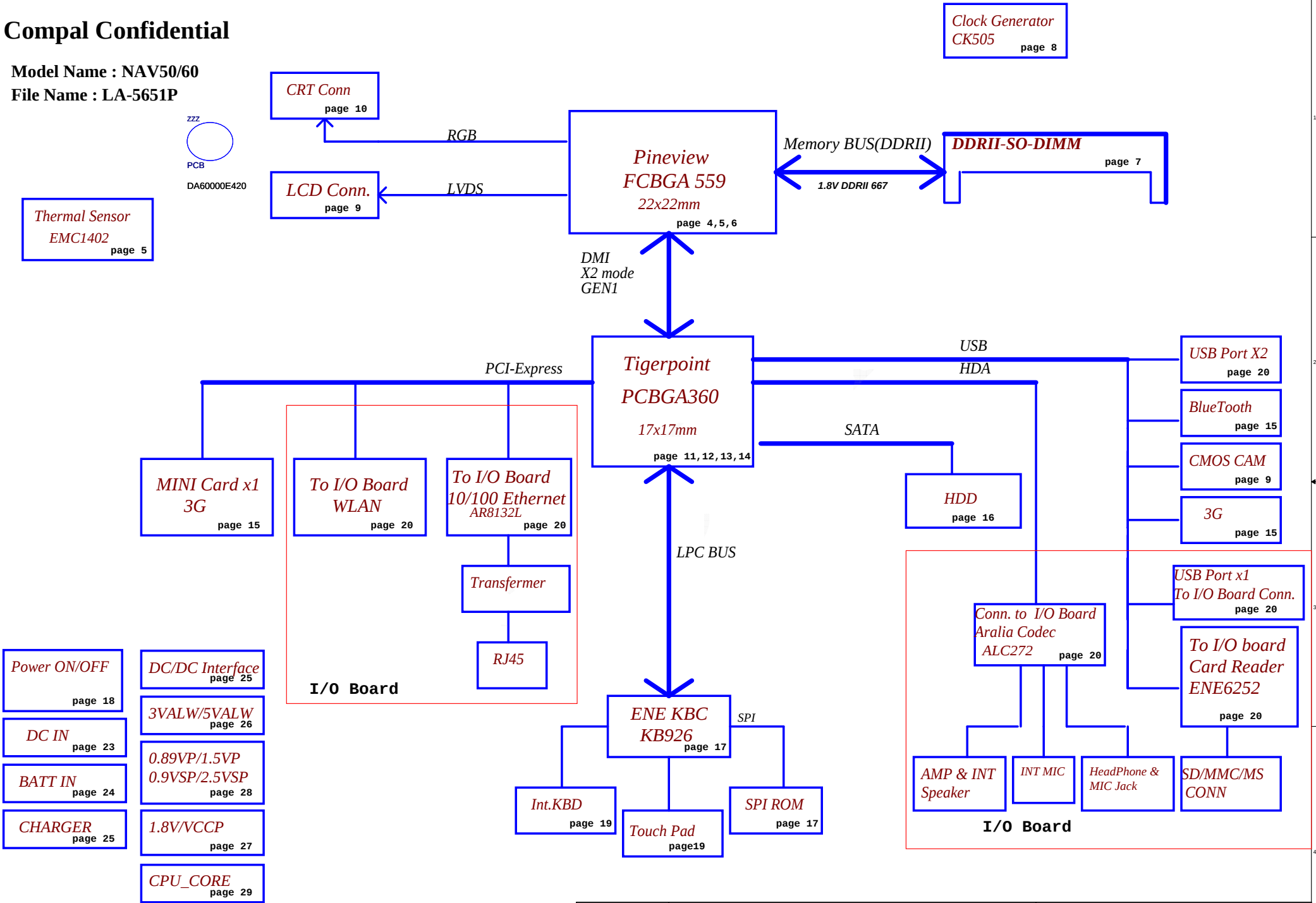
2010 - 05 - 11

REV: 3.0

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				18	401793	D
				Date:	Friday, May 21, 2010	Sheet 1 of 32

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Model Name : NAV50/60
File Name : LA-5651P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

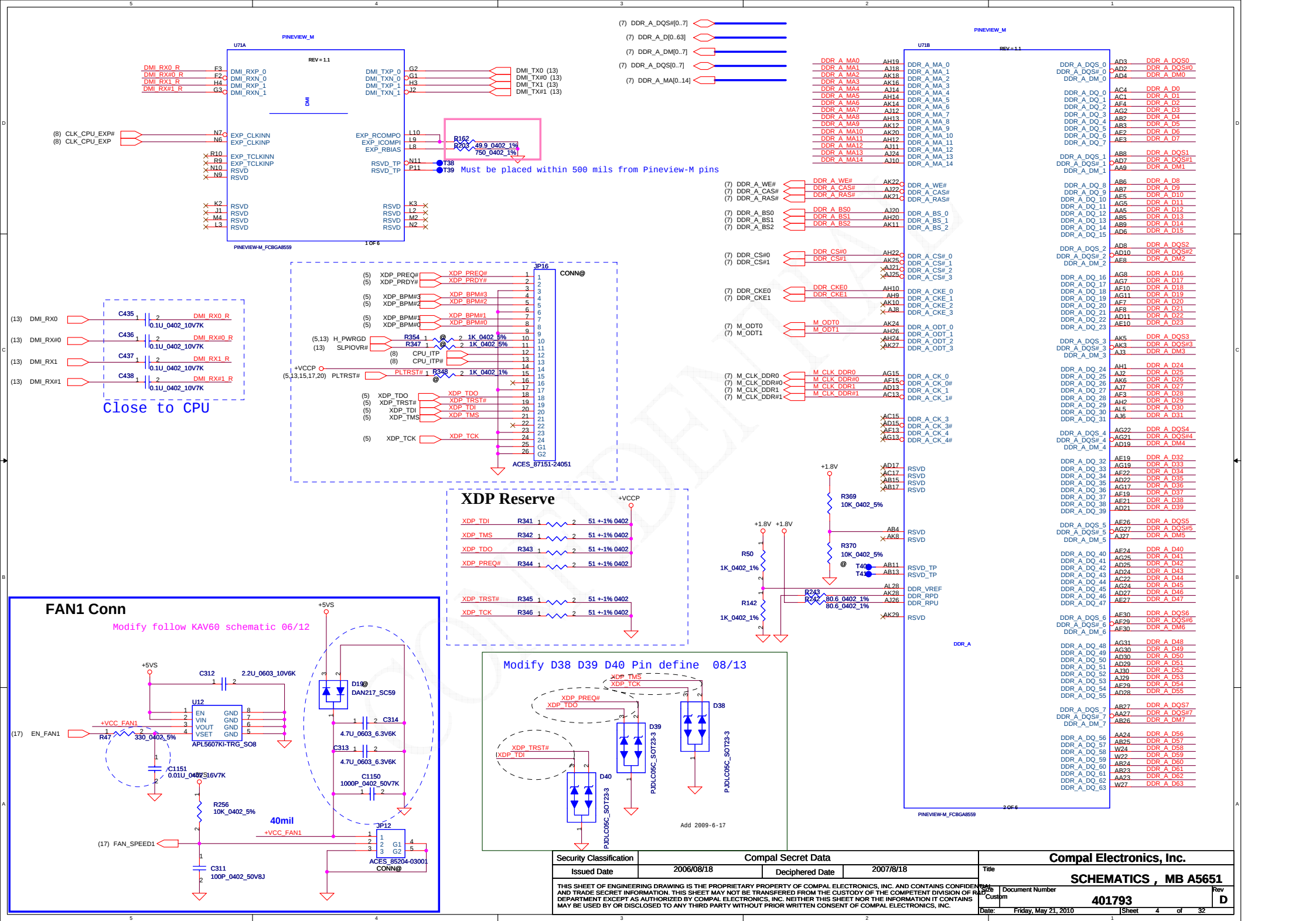
EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb



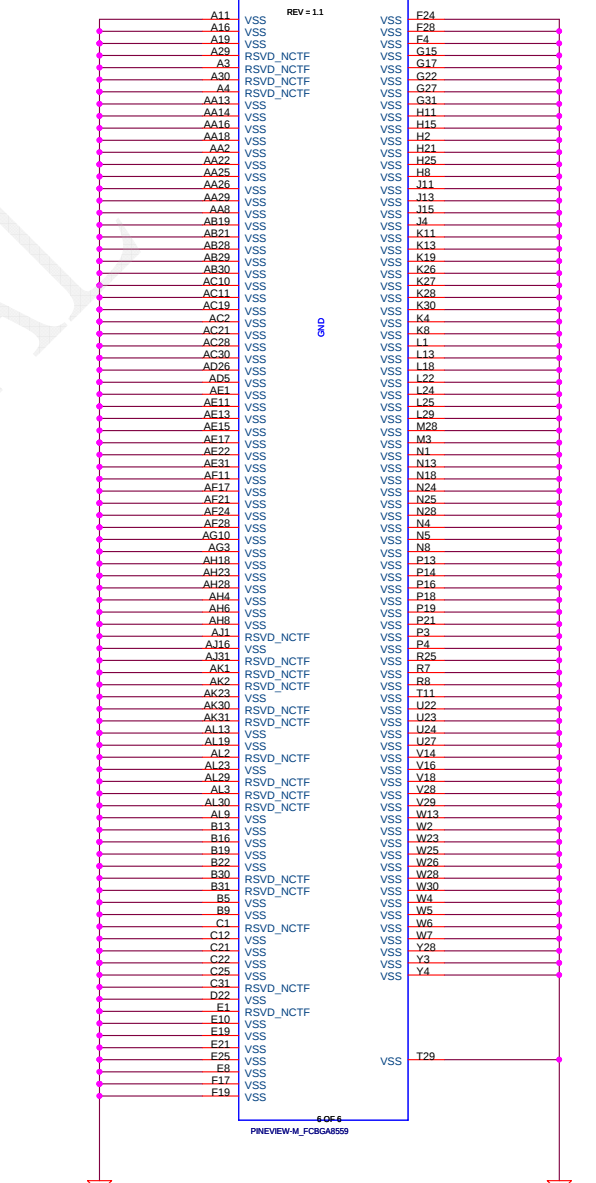
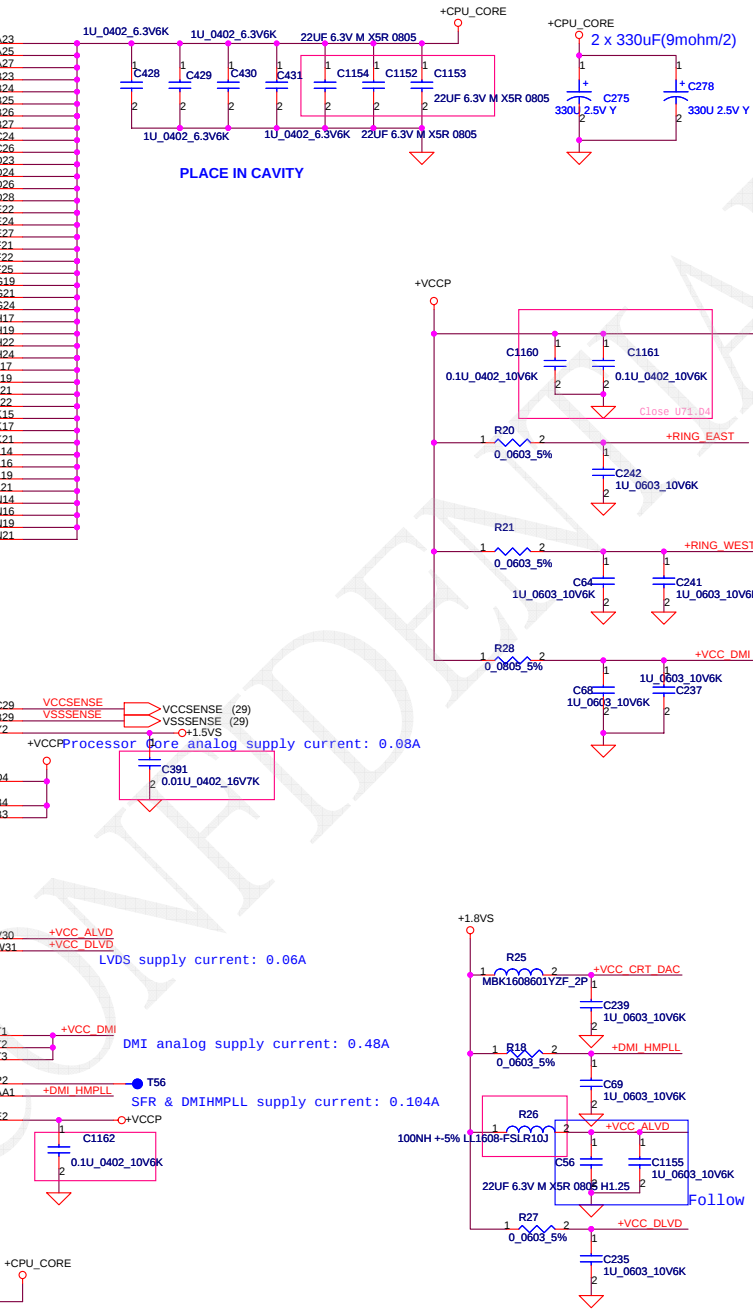
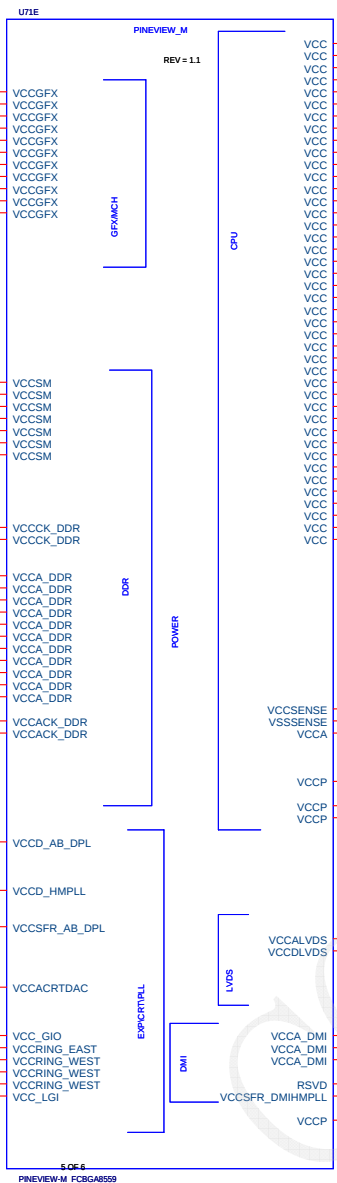
GFX supply current: 1.38A
Sustained GFX supply current: 1.05A

DDR supply current 2.27A

Display PLL SFR and CRT DAC supply current: 0.154A

DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A

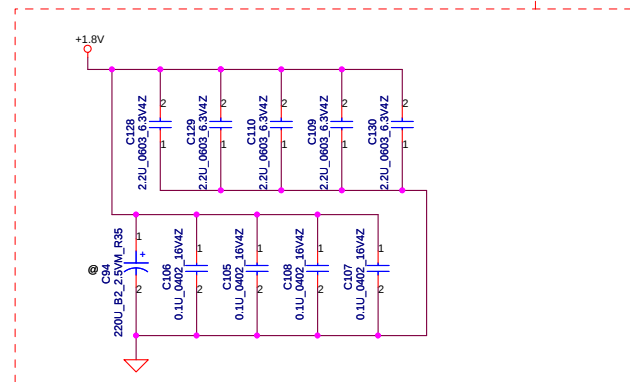
Modify to 2.2u 05/11



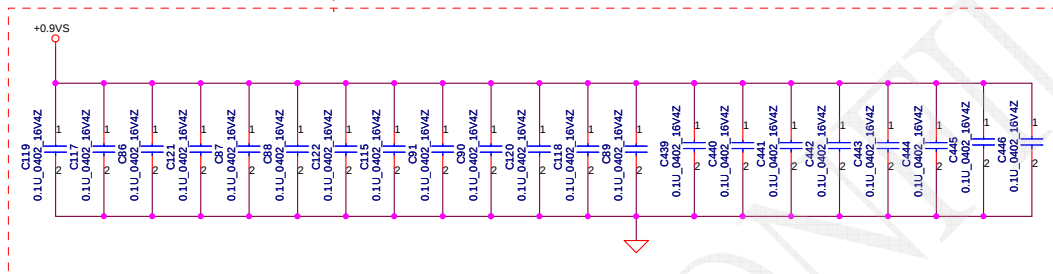
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(4) DDR_A_DQS#[0..7]
(4) DDR_A_D[0..63]
(4) DDR_A_DM[0..7]
(4) DDR_A_DQS[0..7]
(4) DDR_A_MA[0..14]

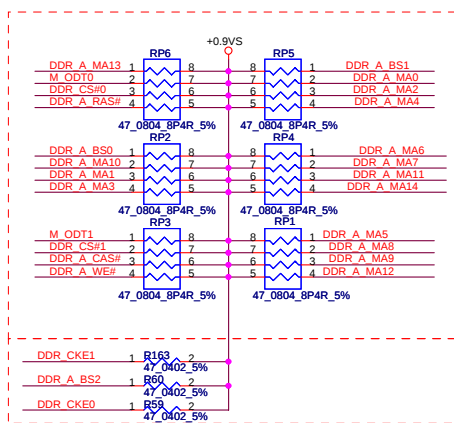
Layout Note:
Place near JDIM1



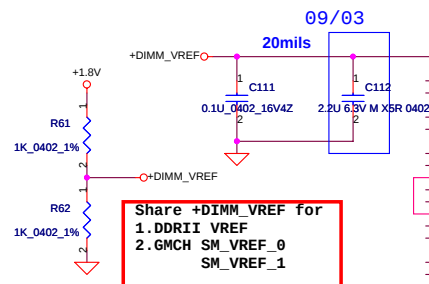
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely DIMMA, all
trace length < 750 mil



Layout Note:
Place these resistor
closely DIMMA, all
trace length
Max=1.3"

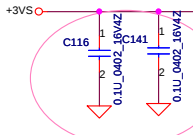


Share +DIMM_VREF for
1. DDRII VREF
2. GMCH SM_VREF_0
SM_VREF_1

(4) DDR_CKE0
(4) DDR_A_BS2
(4) DDR_A_BS0
(4) DDR_A_WE#
(4) DDR_A_CAS#
(4) DDR_CS#1
(4) M_ODT1

DDR A D0
DDR A D1
DDR A DQS#0
DDR A DQS0
DDR A D2
DDR A D3
DDR A D8
DDR A D9
DDR A DQS#1
DDR A DQS1
DDR A D10
DDR A D11
DDR A D16
DDR A D17
DDR A DQS#2
DDR A DQS2
DDR A D18
DDR A D19
DDR A D24
DDR A D25
DDR A DM3
DDR A D26
DDR A D27
DDR_CKE0
DDR A BS2
DDR A BS0
DDR A WE#
DDR A CAS#
DDR CS#1
M_ODT1
DDR A D32
DDR A D33
DDR A DQS#4
DDR A DQS4
DDR A D34
DDR A D35
DDR A D40
DDR A D41
DDR A DM5
DDR A D42
DDR A D43
DDR A D48
DDR A D49
DDR A DQS#6
DDR A DQS6
DDR A D50
DDR A D51
DDR A D56
DDR A D57
DDR A DM7
DDR A D58
DDR A D59
(8,15) CLK_SMBDATA
(8,15) CLK_SMBCLK

Follow Intel Layout checklist, add C141 05/12

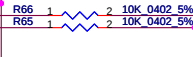


DIMMA

Change to SP07F001720 04/30

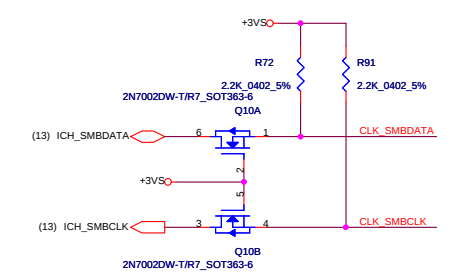


DDR A D4
DDR A D5
DDR A DM0
DDR A D6
DDR A D7
DDR A D12
DDR A D13
DDR A DM1
M_CLK_DDR0
M_CLK_DDR#0
DDR A D14
DDR A D15
DDR A D20
DDR A D21
DDR A DM2
DDR A D22
DDR A D23
DDR A D28
DDR A D29
DDR A DQS#3
DDR A DQS3
DDR A D30
DDR A D31
DDR_CKE1
DDR A MA14
DDR A MA11
DDR A MA7
DDR A MA6
DDR A MA4
DDR A MA2
DDR A MA0
DDR A BS1
DDR A BS#
DDR A CAS#
M_ODT0
DDR A MA13
DDR A D36
DDR A D37
DDR A DM4
DDR A D38
DDR A D39
DDR A D44
DDR A D45
DDR A DQS#5
DDR A DQS5
DDR A D46
DDR A D47
DDR A D52
DDR A D53
M_CLK_DDR1
M_CLK_DDR#1
DDR A DM6
DDR A D54
DDR A D55
DDR A D60
DDR A D61
DDR A DQS#7
DDR A DQS7
DDR A D62
DDR A D63

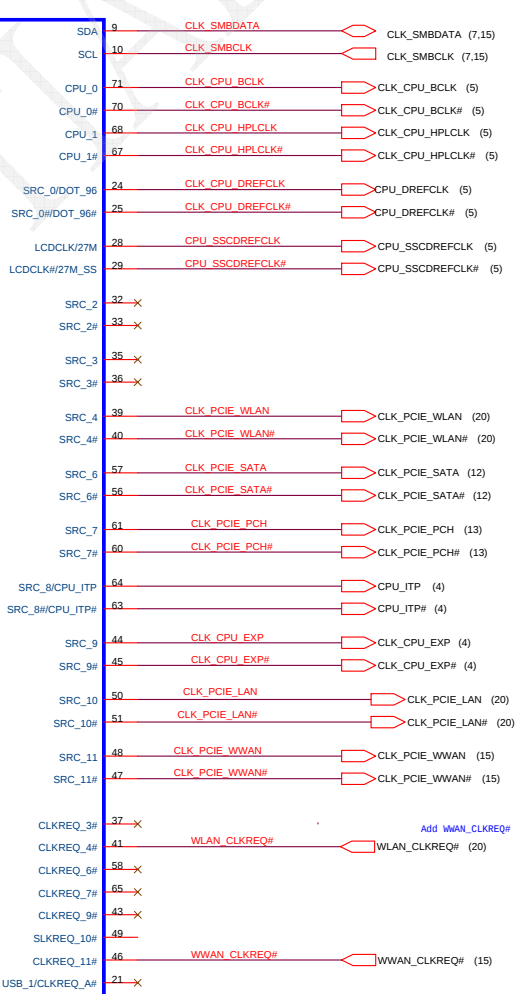
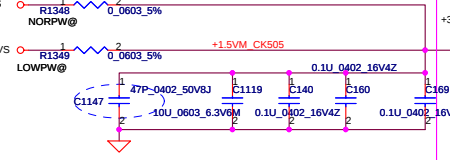


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4	
Change C174 C175 to 10U 0603 05/14	



Change co-lay Low power clock GEN



PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

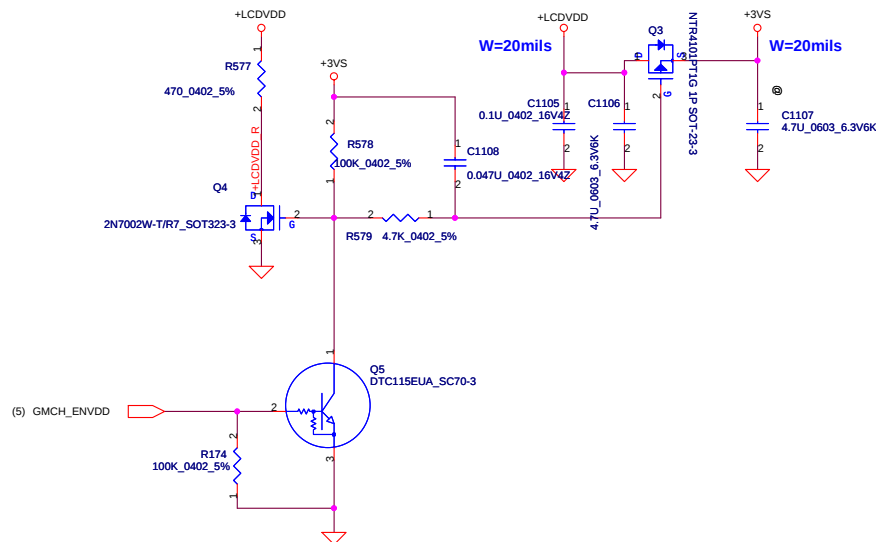
PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	
REQ_11#	PCIE_WWAN
REQ_A#	

Add R107 05/04

WLAN_CLKREQ# R121 2 1 10K 0402 5%

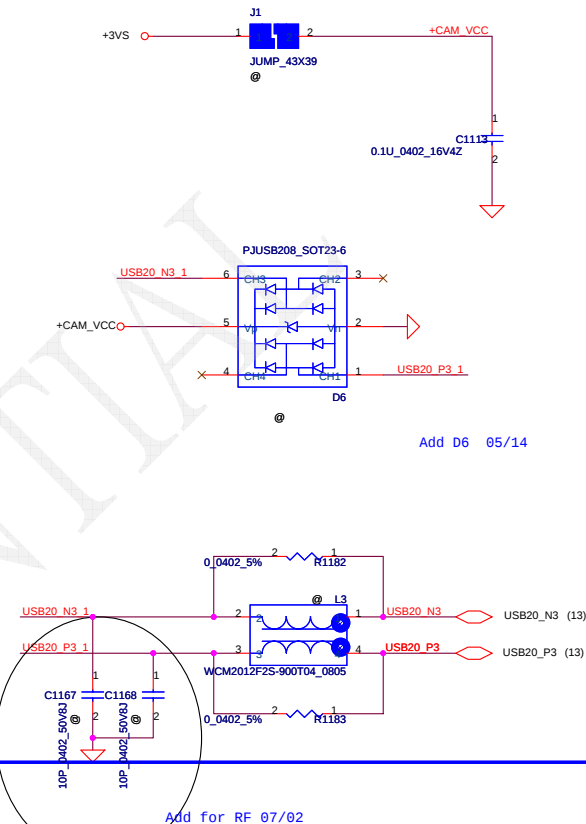
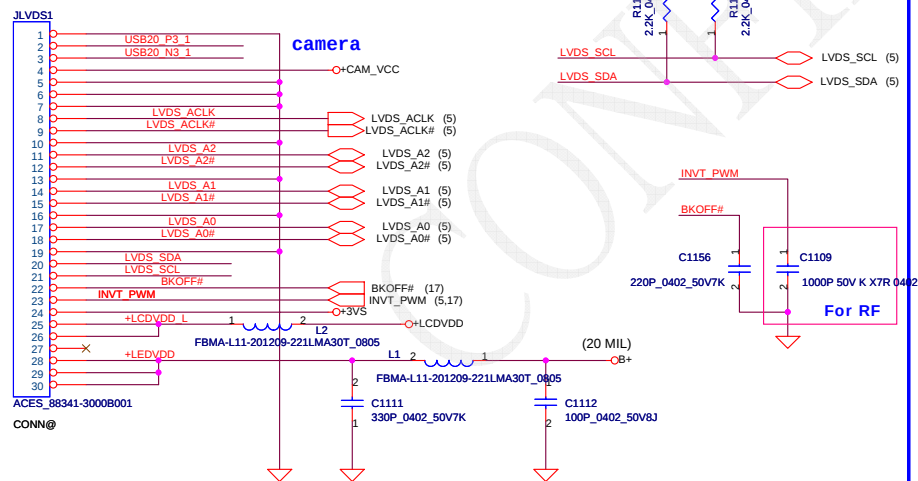
WWAN_CLKREQ# R107 2 1 10K 0402 5%

LCD POWER CIRCUIT

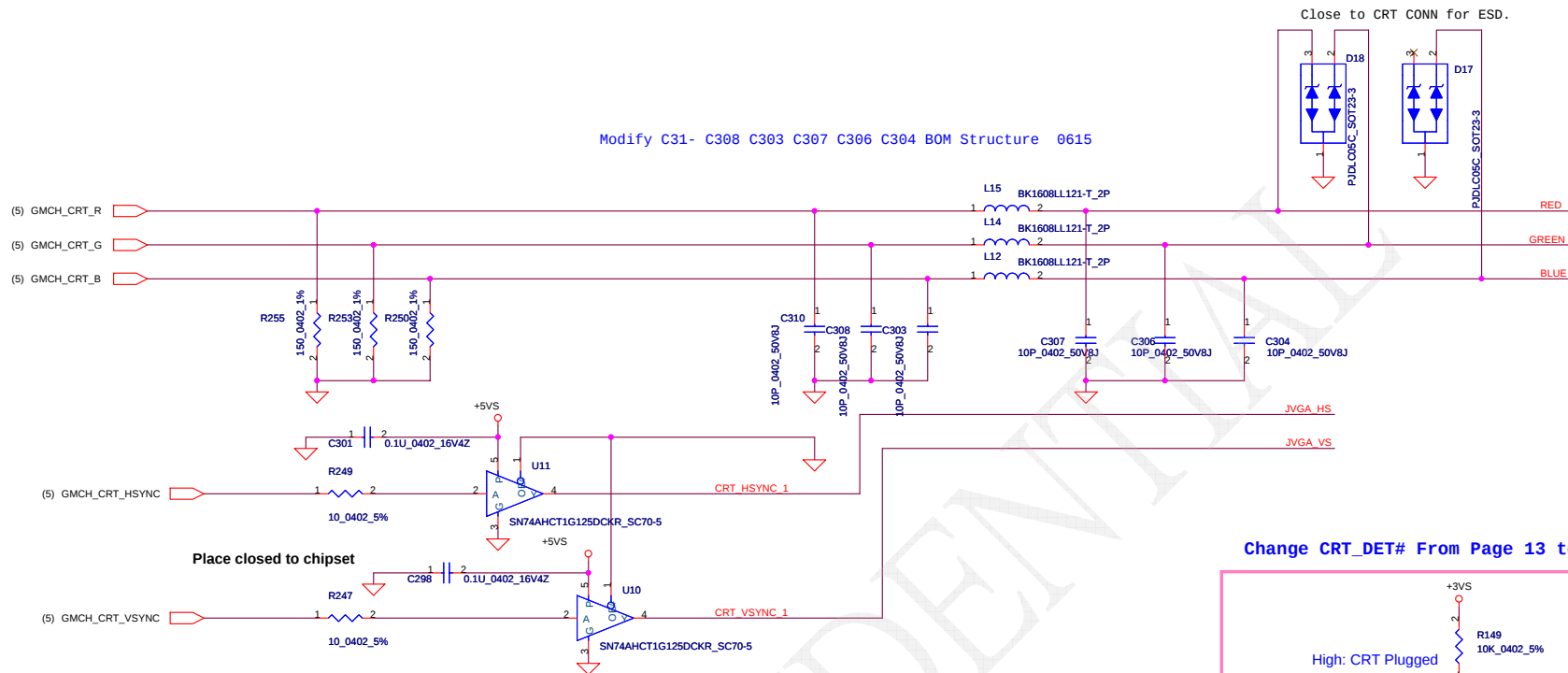


CMOS & LCD/PANEL BD. Conn.

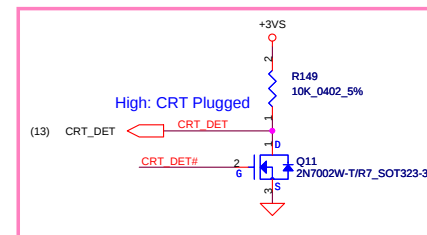
Modify JLVDS1 08/04



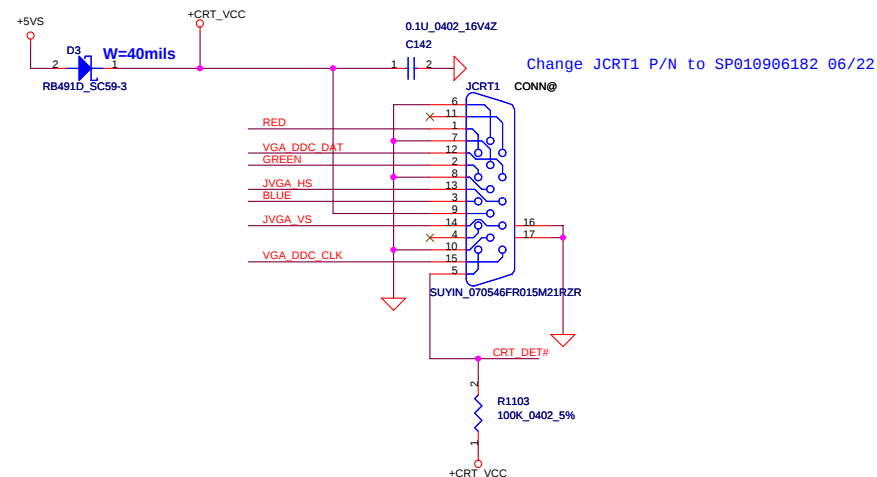
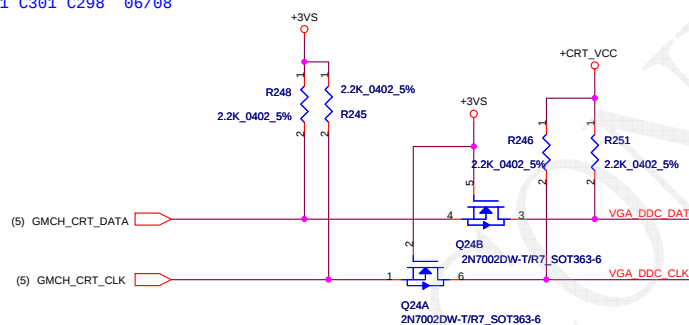
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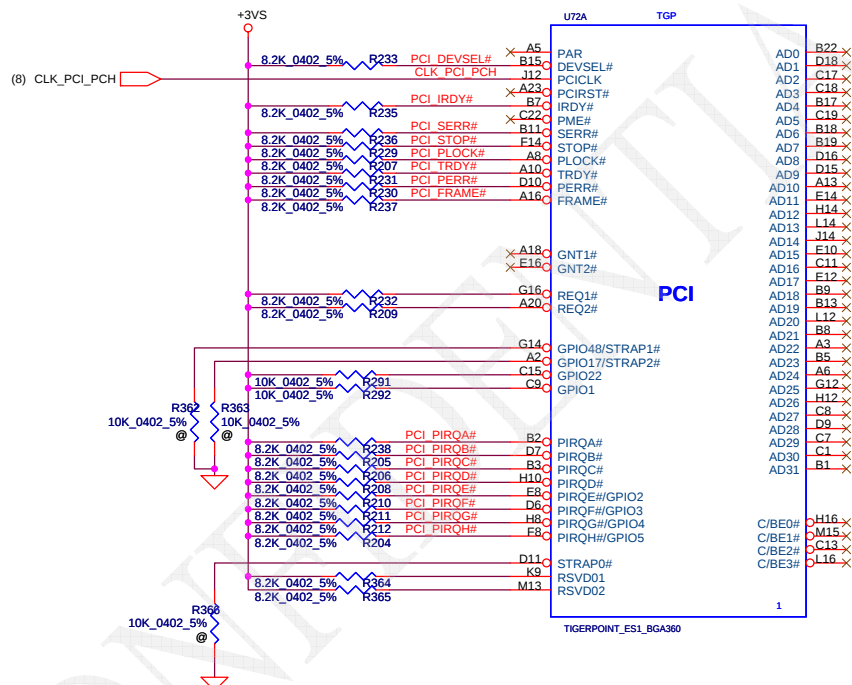
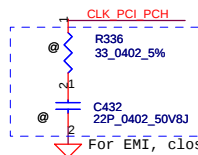
Change CRT_DET# From Page 13 to Page 10 06/12



CRT PORT

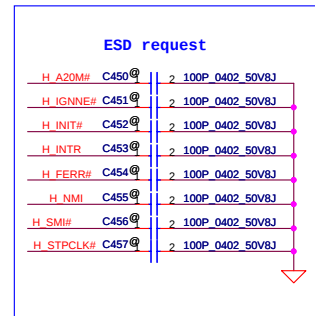
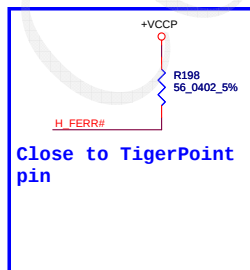
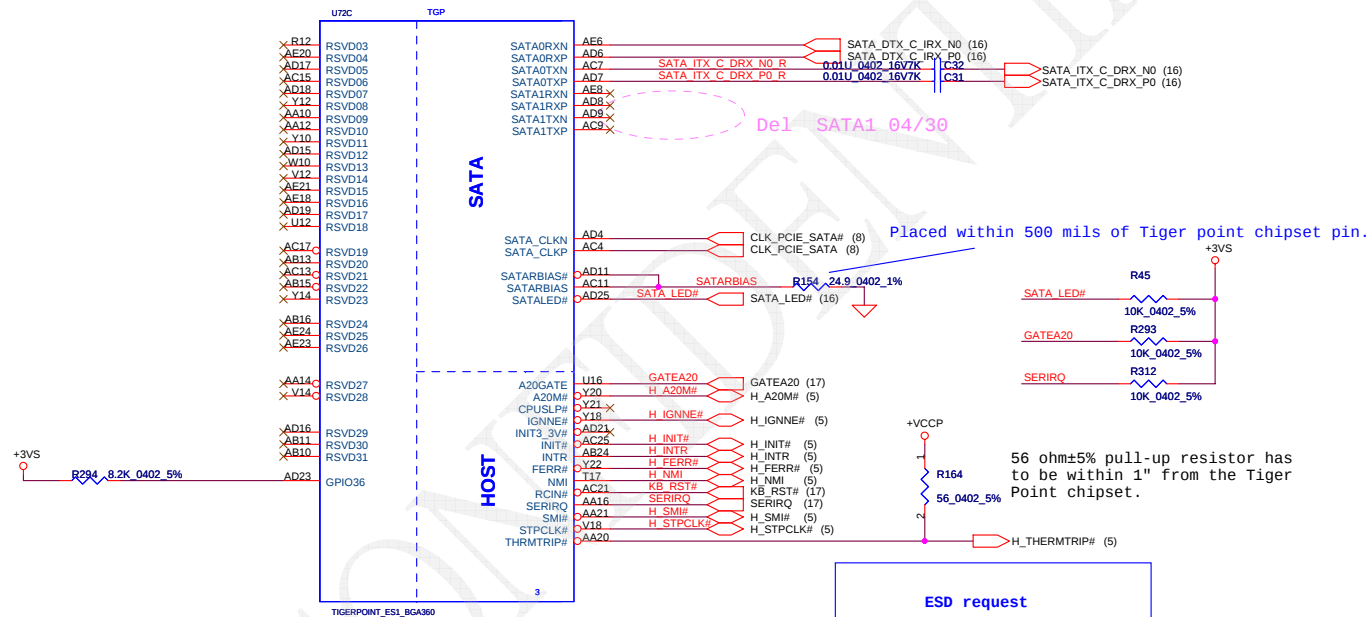


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STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

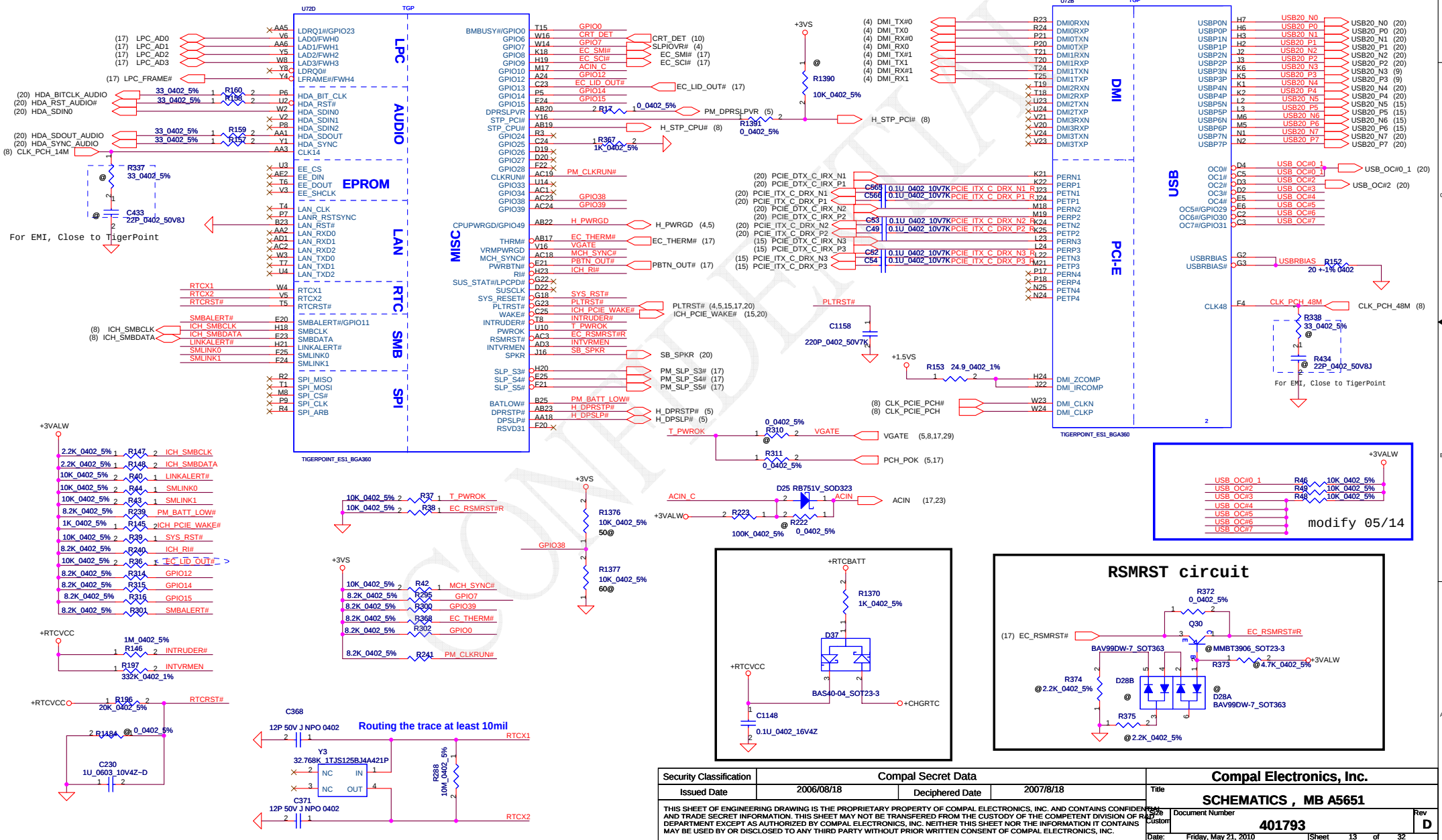
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PCIE Port List	
1	LAN
2	WLAN
3	WWAN
4	

USB Port List	
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



Mini-Express Card for WWAN

(17) EC_TX_P80_DATA R402, 0402_5%
 (17) EC_RX_P80_CLK EC_RX_P80_CLK 1 2 EC_TX_P80_CLK R
 R403 0_0402_5%

Change JMINI1 to FOX_AS08246-S50U-7F_52P-T 06/29

(13,20) ICH_PCIE_WAKE# ICH_PCIE_WAKE#

(8) WWAN_CLKREQ# WWAN_CLKREQ#

(8) CLK_PCIE_WWAN#

(8) CLK_PCIE_WWAN#

(13) PCIE_DTX_C_IRX_N3

(13) PCIE_DTX_C_IRX_P3

Change to PCIE_P3 05/13

(13) PCIE_ITX_C_DRX_N3

(13) PCIE_ITX_C_DRX_P3

+3VS_WWAN

10U 0805 10V4Z

WWAN_WAKEUP_R#

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_VPP

Reserve for SIM card does not meet rise time and pull-up is needed.

Add C1163 C1164 C1165 C1166 06/23

Add C850 06/12

Close to WWAN CONN

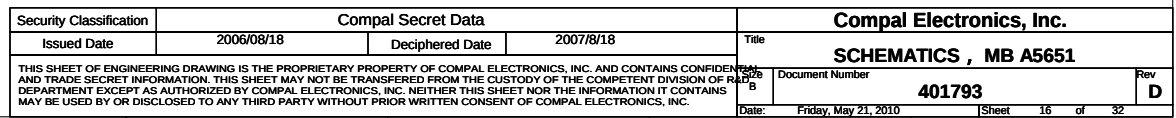
(9~16mA)

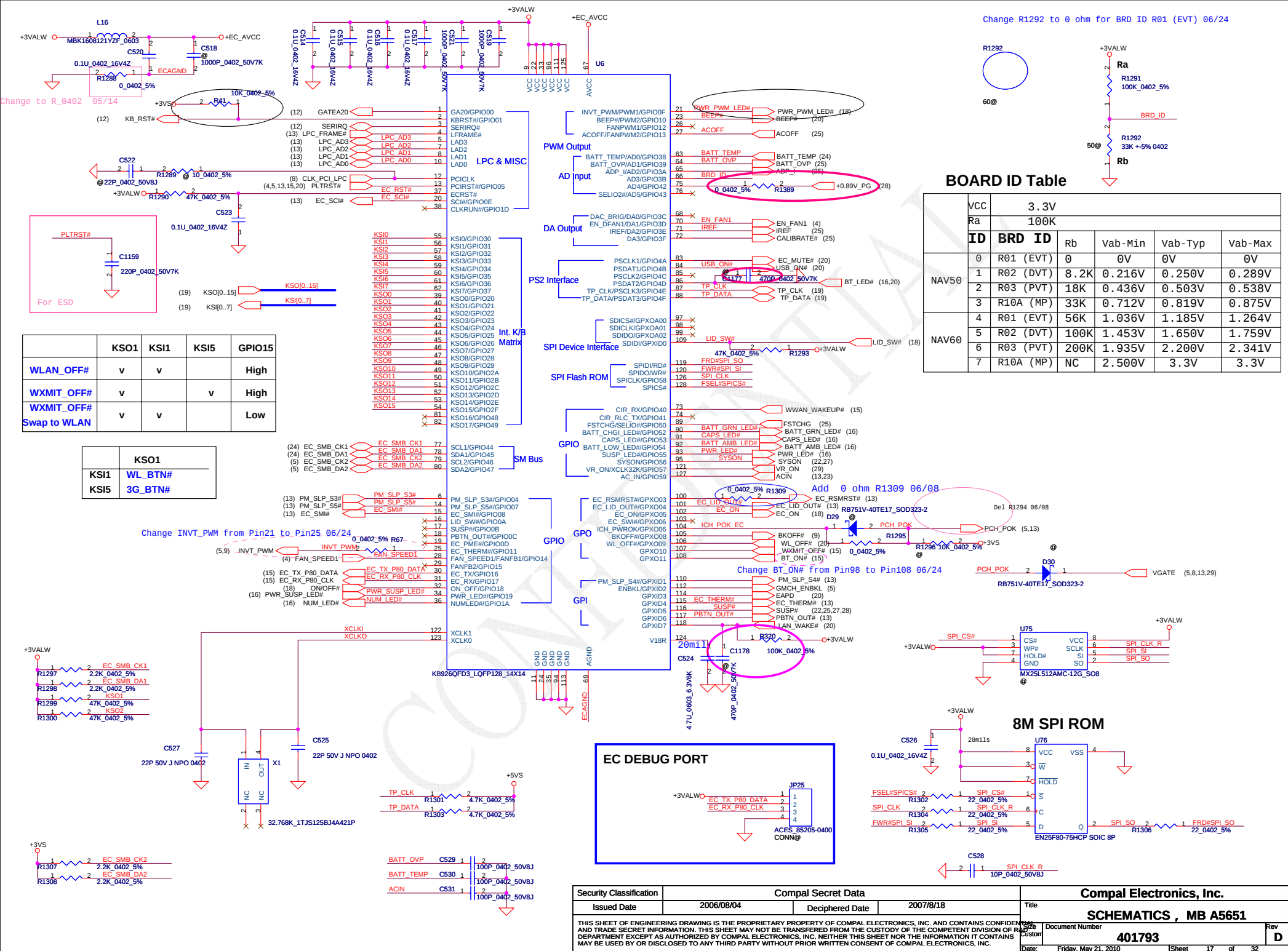
BT MODULE CONN

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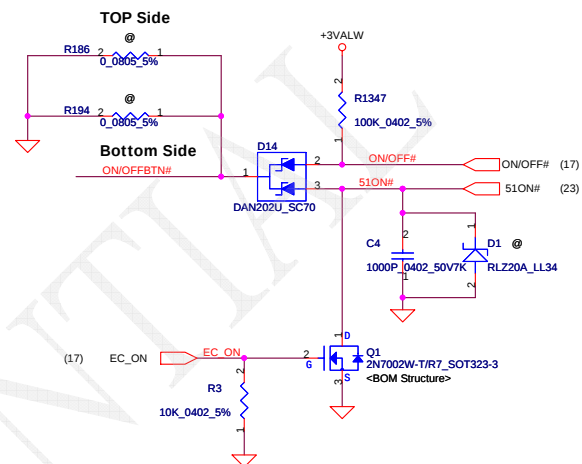
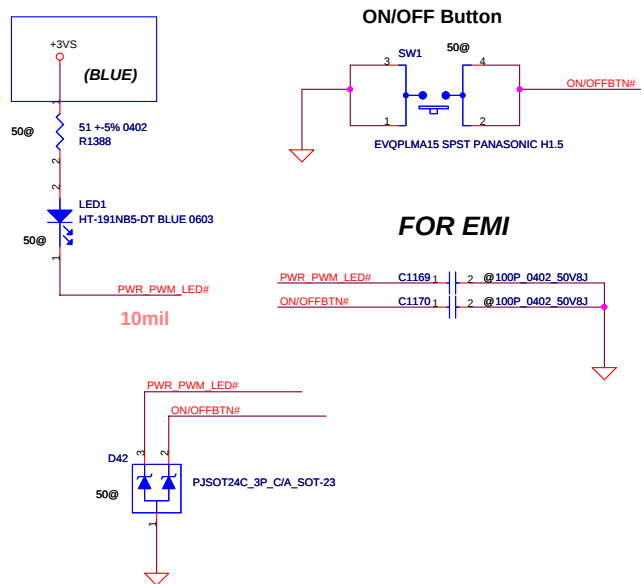
LED PCB CONN

09/03 Change +5VALW , +5VS to +3VALW +3VS

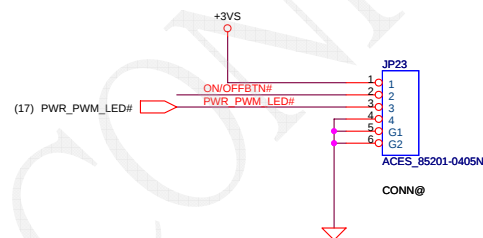




Add For NAV50 07/06
09/03 Change +5VS to +3VS

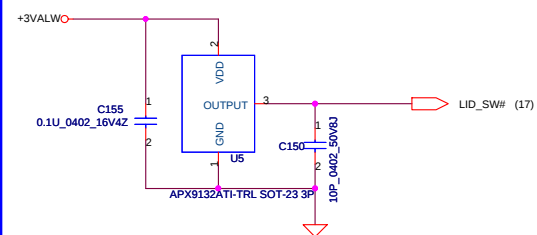


PWR/B Conn

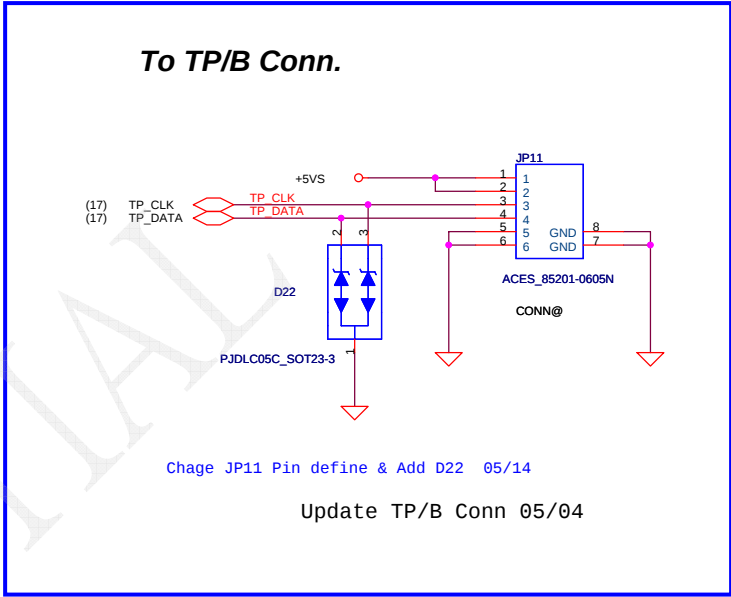
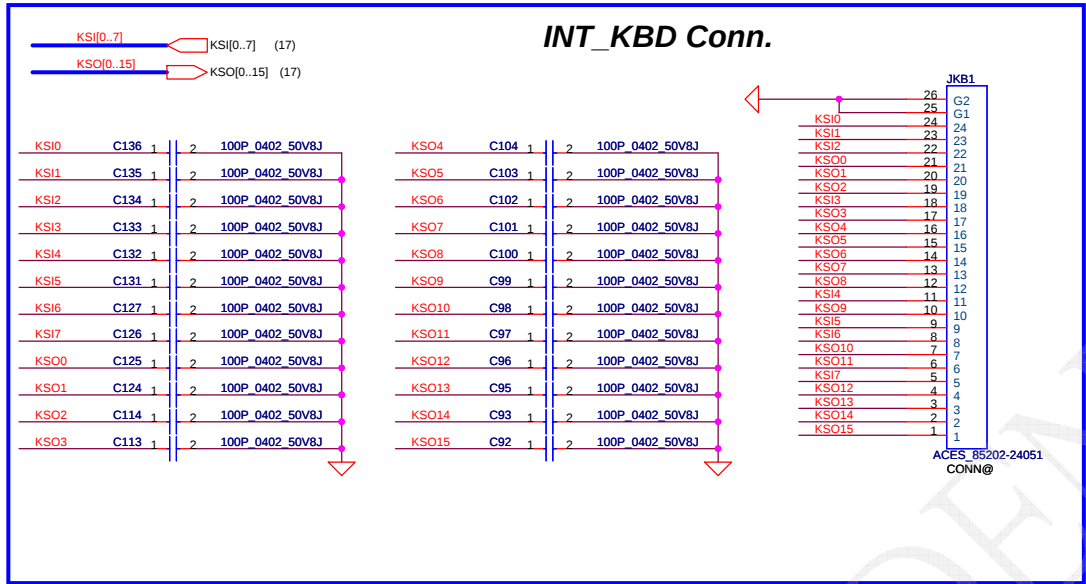


Update PW/B Conn 0623

LID Switch

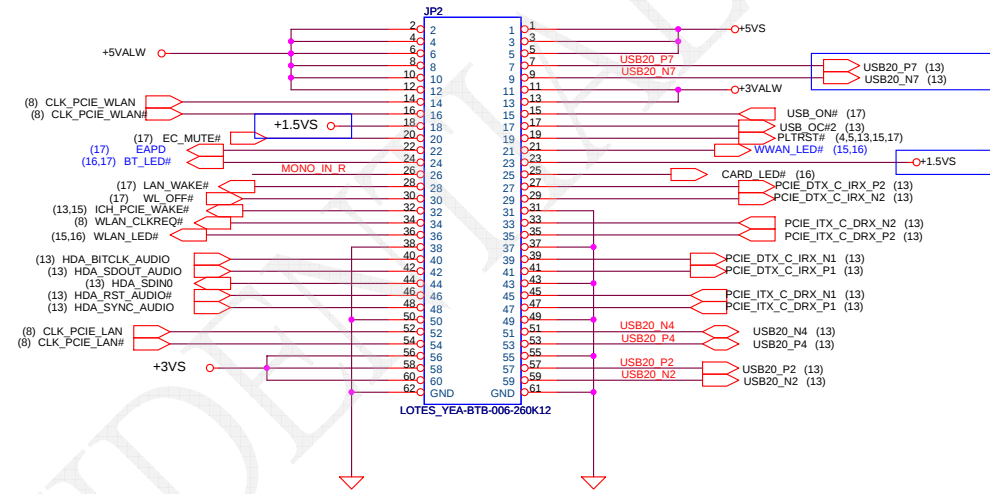
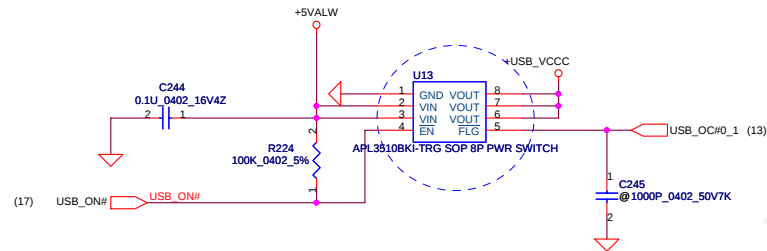
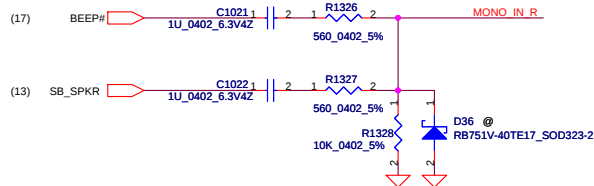


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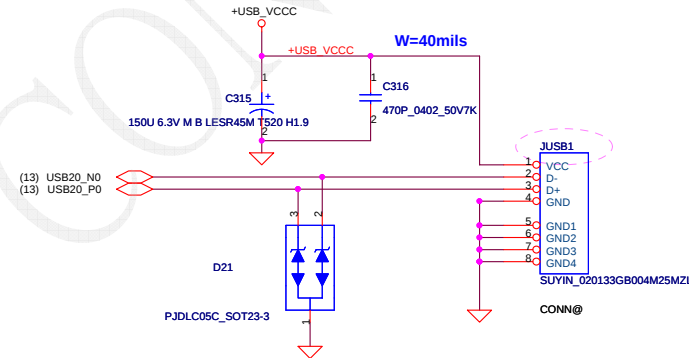


09/03 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7

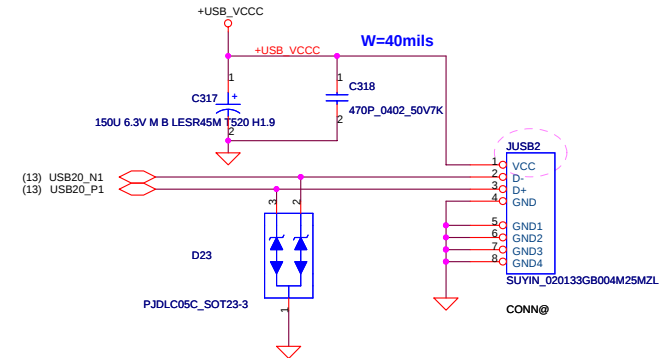
I/O Board Conn.



USB CONN.1

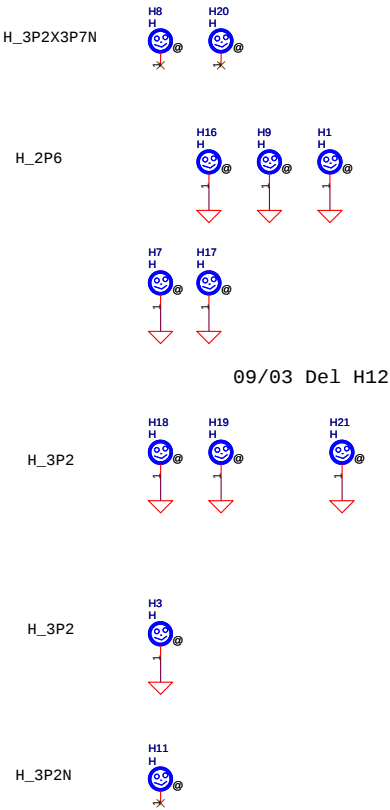


USB CONN.2



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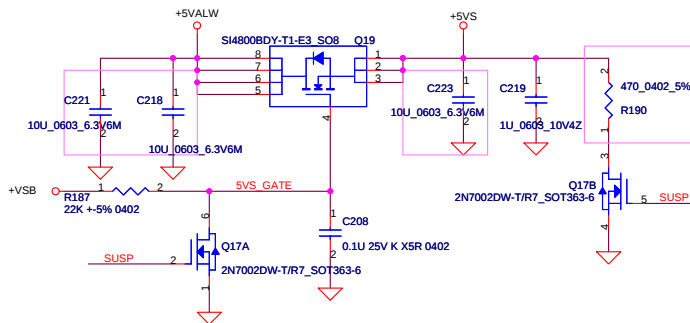
Modify Hole location by (ME Drawing 06/12) 0615



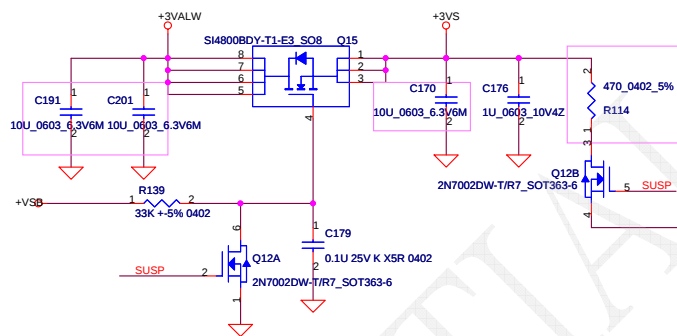
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30
 Change C221 C218 C223 C 191 C170 C392 C393 C394 to 0603 SIZE 04/30

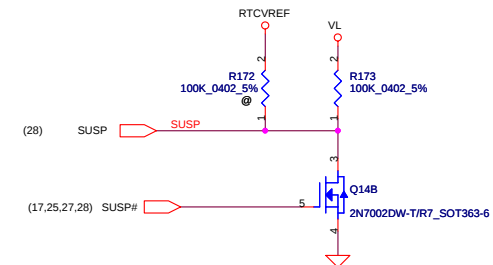
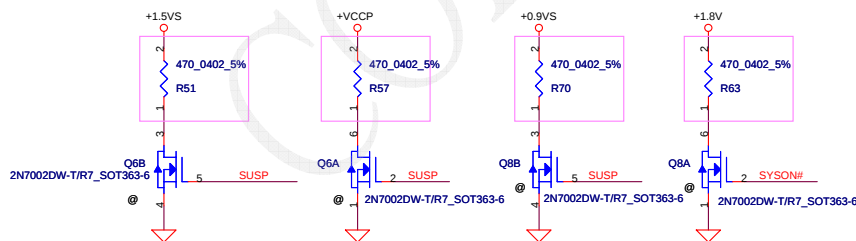
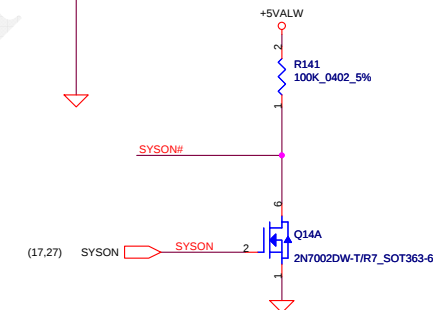
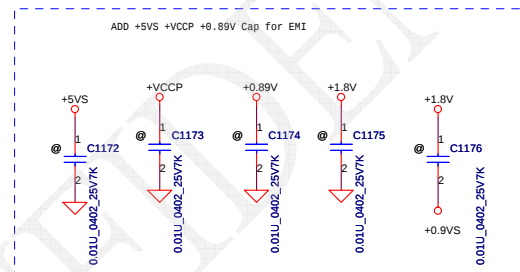
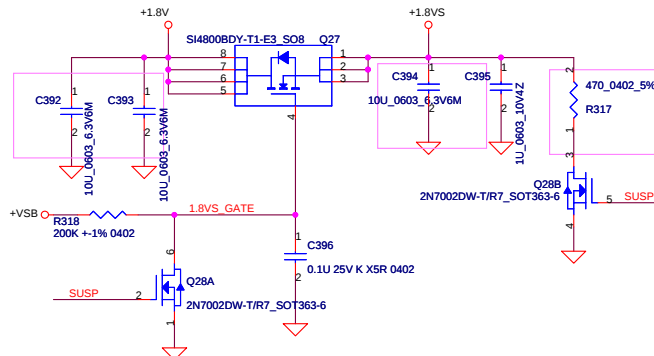
+5VALW TO +5VS



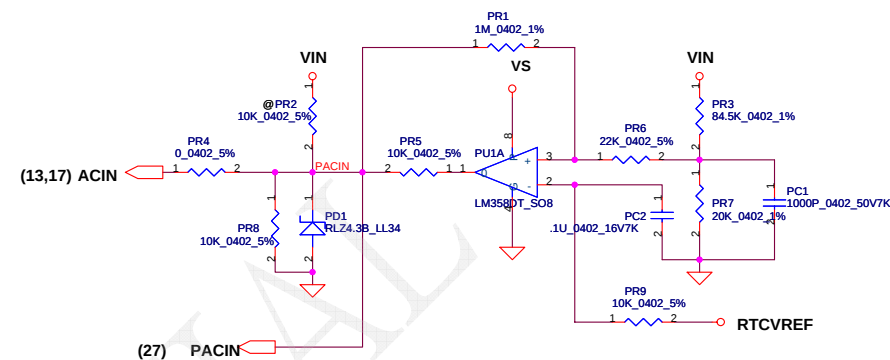
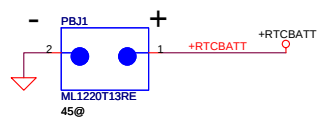
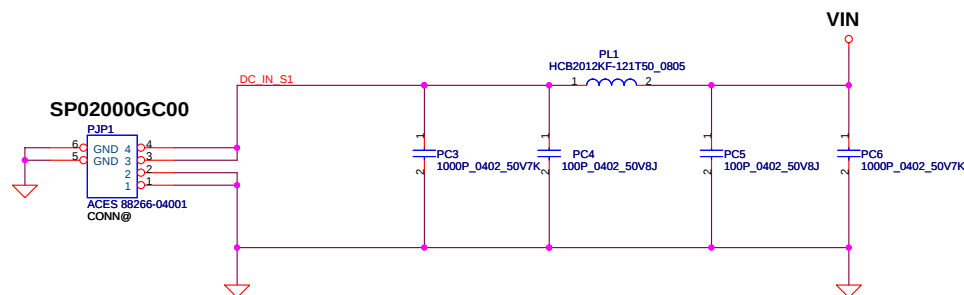
+3VALW TO +3VS



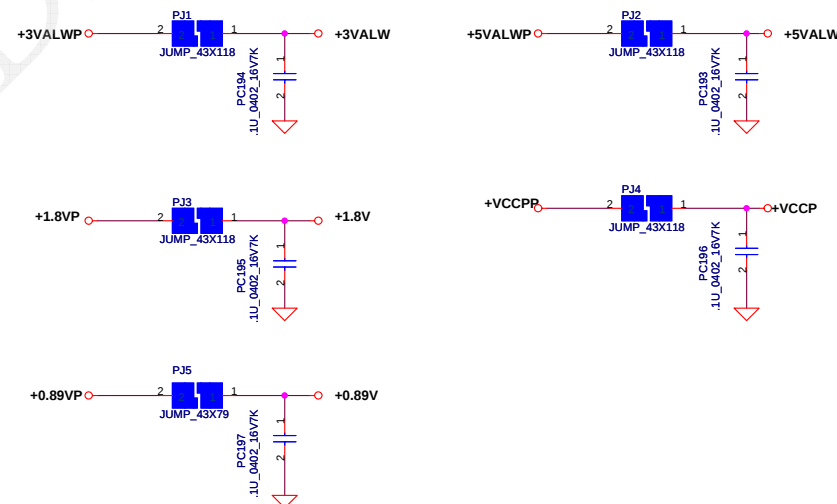
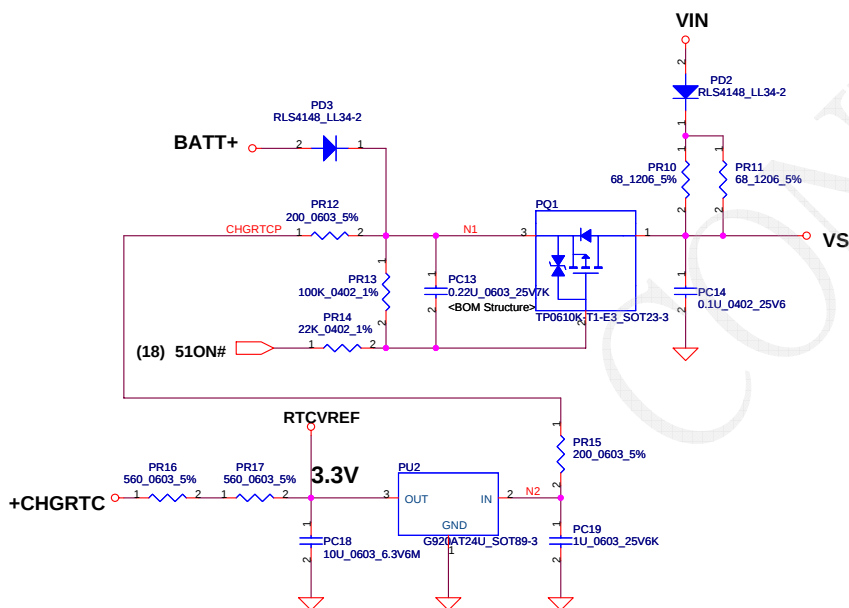
+1.8V to +1.8VS



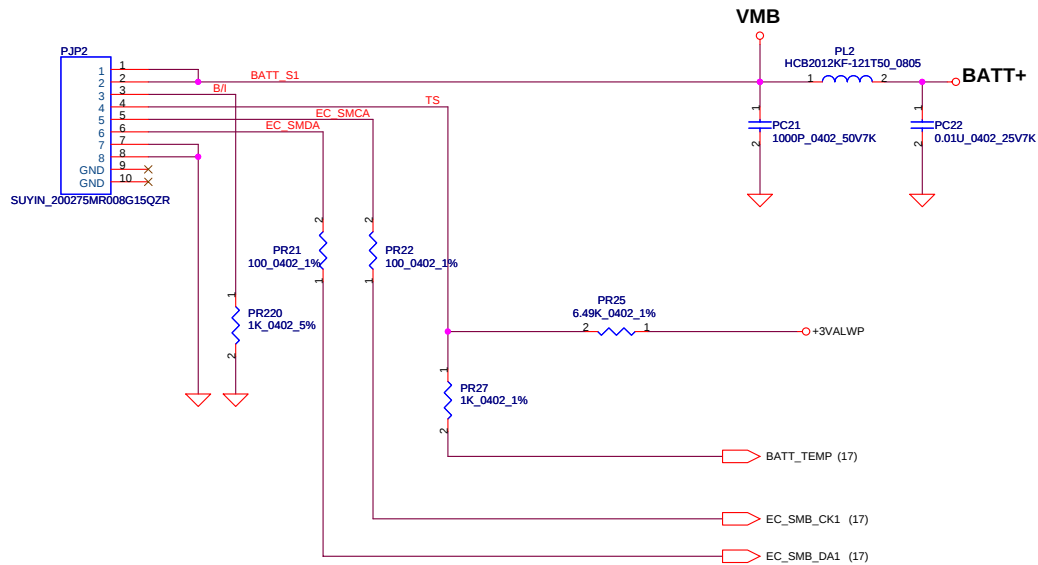
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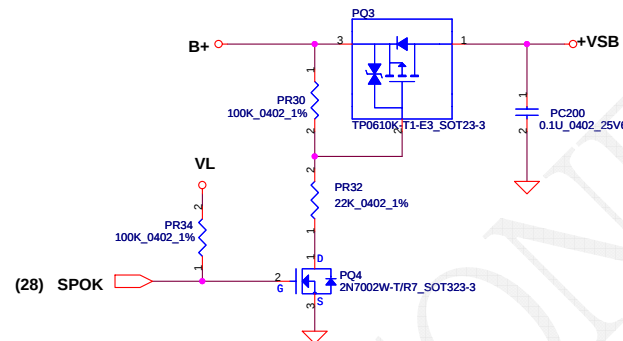
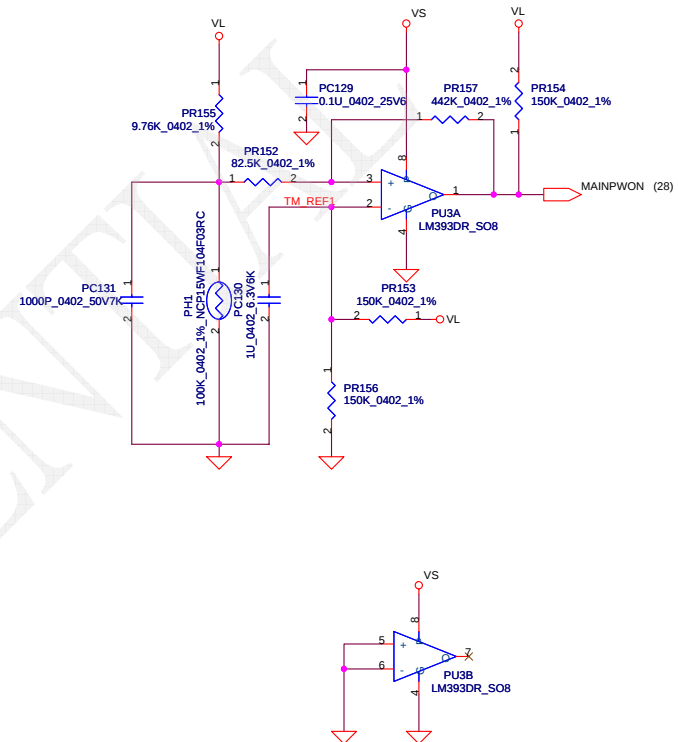
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



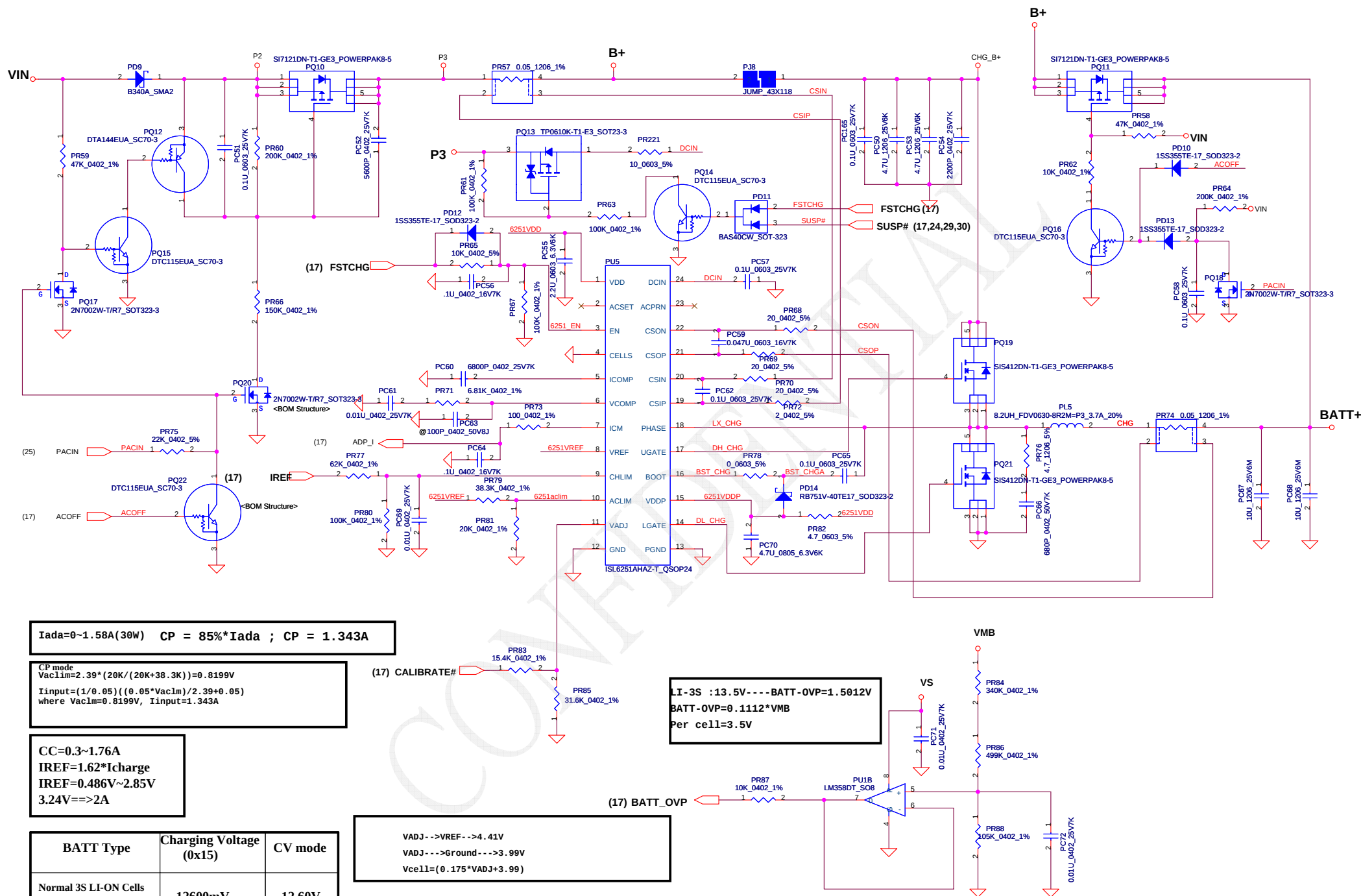
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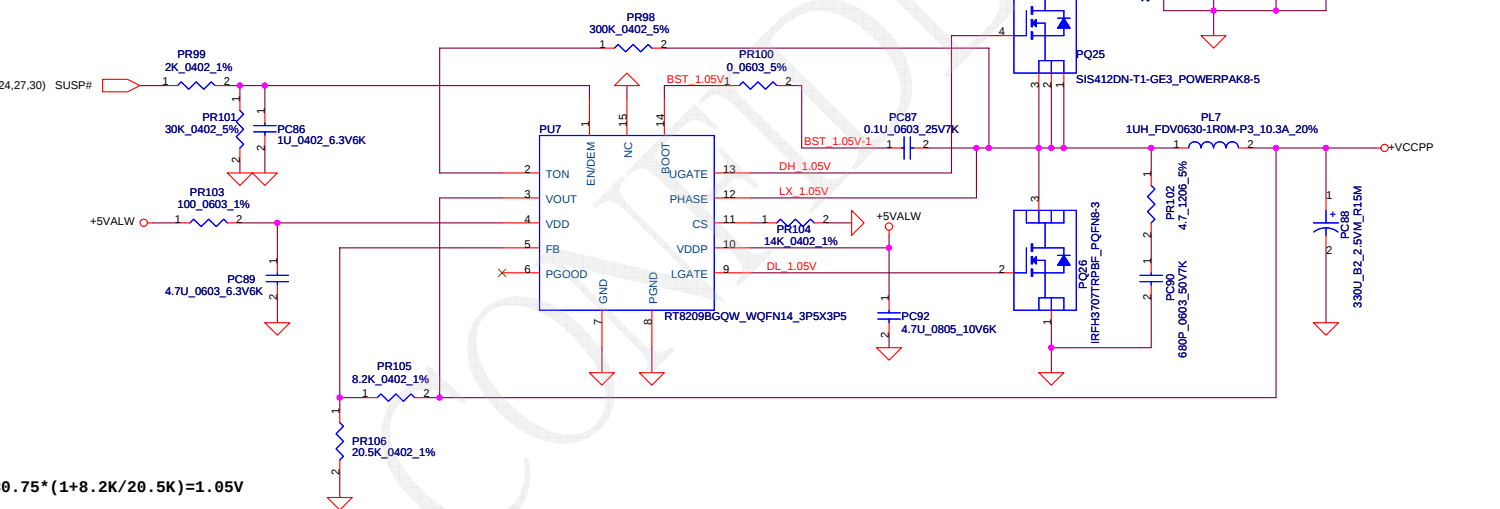


PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



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```

VVo=1.8V; VVB=0.75V
Vo=VVB*(1+PR96/PR97)=0.75*(1+28.7K/20.5K)=1.8V
FSW=328KHz

Cout ESR=15m ohm Rdsn(max)=17.9m Rdsn(typical)=14.5m
Ipeak=4.97A, Imax=3.479A, Iocp=5.964A
Delta I=((19-1.8)*(1.8/19))/(2.2u*328K)=2.259A
=>1/2DeltaI=1.129A
Vtrip=Rtrip*10uA=8.66K*10uA=0.0866V
Iocpmin=Vtrip/(Rdsnmax)*1.129
=0.0866/(0.0179)+1.129=5.967A
Iocpmax=(0.0866/(0.0145*1.2))+1.129=6.106A
Iocp=5.967A-6.106A

```

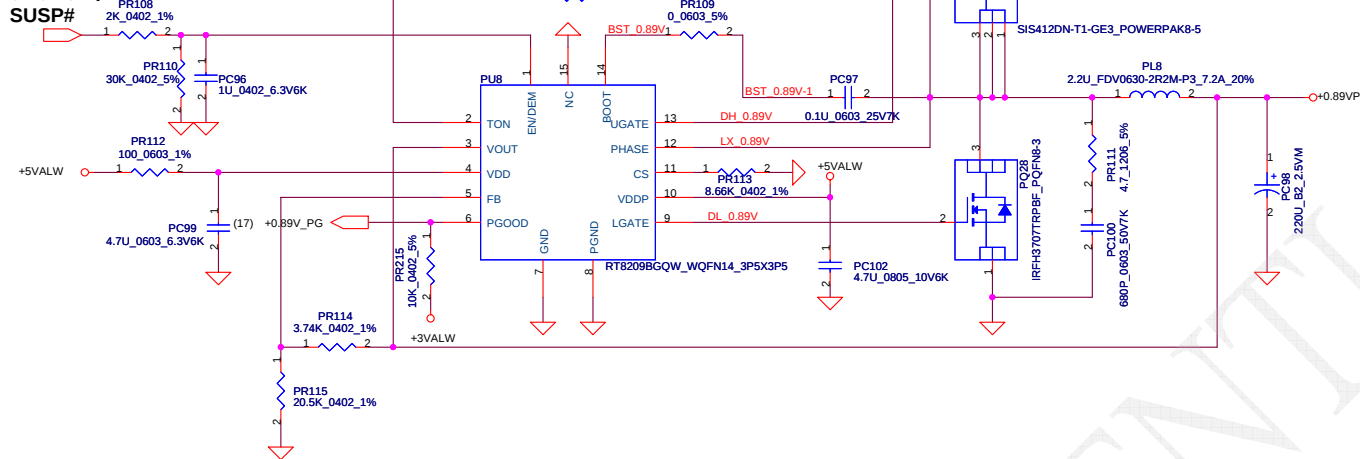
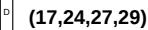
```

<Vo=-1.05V>      VFB=0.75V
<Vo=VFB*(1+PR105/PR106)=0.75*(1+8.2K/20.5K)=1.05V
FSW=280KHZ

Cout ESR=15m ohm Rdson(max)=17.9m  Rdson(typical)=14.5m
Ipeak=3.124A, Imax=2.187A, Iocp=3.749A
Delta I=(19-1.05)*(1.05/19))/(1.5u*280K)=3.549A
=>1/2DeltaI=1.774A
Vtrip=Rtrip*10uA=14K*10uA=0.14V
Iocpmin=Vtrip/(Rdsonmax)+1.774
=0.14/(0.0179)+1.774=9.596A
Iocpmax=(0.14/(0.0145*1.2))+1.774=9.820A
Iocp=9.596A-9.820A

```

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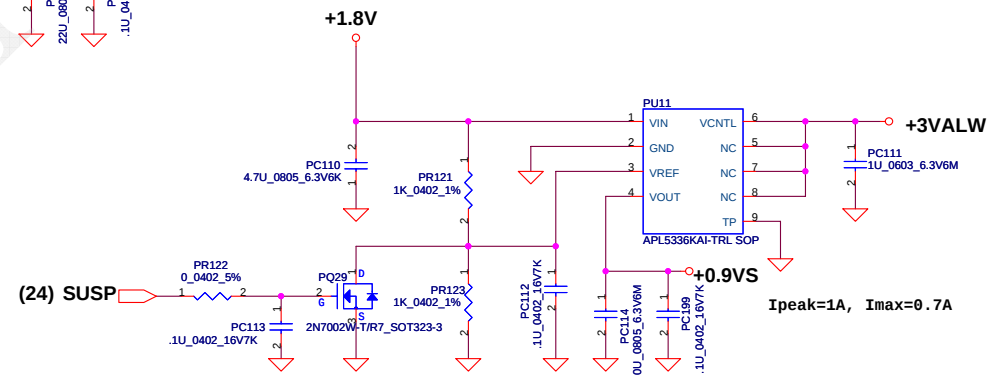
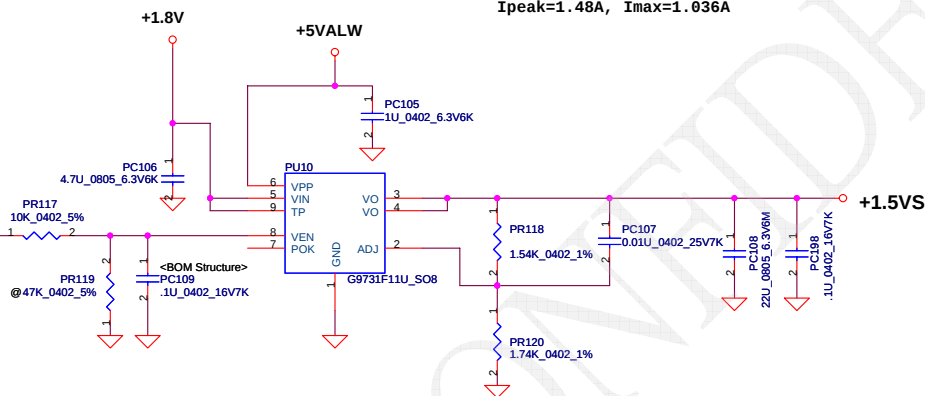
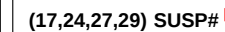
<Vo=0.89V> VFB=0.75V
 $V_o = V_{FB} * (1 + PR_{114} / PR_{115}) = 0.75 * (1 + 28.7K / 20.5K) = 0.89V$
 Fsw=263KHz

```

Cout ESR=15m ohm Rds(on)(max)=17.9m Rds(on)(typical)=14.5m
Ipeak=1.38A, Imax=0.966A, Iocp=1.656A
Delta I=(-(19-1.8)*(1.8/19))/(2.2u*263K)=1.467A
=>1/2DeltaI=0.7335A
Vtrip=Rtrip*10uA=0.66K*10uA=0.0866V
Iocpmin=Vtrip/(Rds(on)max)+0.7335
=0.0866/(0.0179)+0.7335=5.572A
Iocpmax=(-0.0866/(0.0145*1.2))+0.7335A=5.711A
Iocp=5.572A-5.711A

```

I_{peak}=1.48A, I_{max}=1.036A



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Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	add PC200	For design change	0.1	24		2009.5.15	EVT
2	add PC193,PC194	For design change	0.1	26		2009.5.15	EVT
3	add PC195,PC196	For design change	0.1	27		2009.5.15	EVT
4	add PC197,PC198,PC199	For design change	0.1	28		2009.5.15	EVT
5	change PL3,PL4	For design change	0.1	26	change PL3,PL4 to 4.7uH	2009.5.15	EVT
6	change PQ10,PQ11	For design change	0.1	25	change PQ10,PQ11 to P-Chanel	2009.6.5	EVT
7	add PC165	Solution for 3G noise reduce	0.1	25		2009.6.5	EVT
8	add PC163,PC164	Solution for 3G noise reduce	0.1	26		2009.6.5	EVT
9	add PC166,PC167	Solution for 3G noise reduce	0.1	27		2009.6.5	EVT
10	add PC168	Solution for 3G noise reduce	0.1	28		2009.6.5	EVT
11	delete PC103,PC1120	For design change	0.1	29		2009.6.5	
12	change PR94,PR102	For design change	0.1	27	change PR94,PR102 to 100ohm	2009.6.5	
13	change PC79,PC89	For design change	0.1	27	change PC79,PC89 to 4.7uF	2009.6.5	
14	change PR112	For design change	0.1	28	change PR112 to 100ohm	2009.6.5	
15	change PC99	For design change	0.1	28	change PC99 to 4.7uF	2009.6.5	
16	change +5VALW/+3VALW OCP	For design change	0.1	26	change PR49 to 309ohm & PR50 to 249ohm	2009.6.5	
17	add PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7	For design change	0.1	25		2009.6.15	
18	add PJ9,PJ10	For design change	0.1	28		2009.6.15	
19	Change net name	For design change	0.1	25	Change net name +1.05V to +VCCP	2009.6.15	
20	Change PJP2	For design change	0.1	24	Change PJP2 to DC040903020	2009.6.15	
21	Change PBJ1	For design change	0.1	23	Change PBJ1 to SP020008Y00	2009.6.15	
22	delete PJ6,PJ7,PJ9,PJ10	For design change	0.1	28		2009.6.18	
23	Change net name	For design change	0.1	29	Change net name GND_SIGNAL to GND	2009.6.18	

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Change PR194	For design change	0.1	29	change PR194 to 4.7K ohm	2009.6.30	EVT
2	add PR221	For design change	0.1	25		2009.6.30	EVT
3	Change PR4	For design change	0.1	23	change PR4 to 0 ohm	2009.7.2	EVT
4	Change PJP3 to PBJ1	For design change	0.1	23	change SP020008Y00 to SP093MX000	2009.8.4	EVT
5	Change PH1 & PH4	For design change	0.1	24	change SL210031F00 to SL200000V00	2009.8.12	EVT
6	Change PL10	For design change	0.1	29	change SH000006I80 to SH000000700	2009.8.12	EVT
7	Change PR99 & PR108	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034200280(20K ohm)	2009.8.12	EVT
8	Change PR90	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.12	EVT
9	Change PR83	Modify ISL6251 Charger KV	0.1	25	change SD034182280(18.2 ohm) to SD034154280(15.4K ohm)	2009.8.24	EVT
10	Change PR117	Modify power sequence	0.1	28	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.24	EVT
11	Change PR99 & PR108	Modify power sequence	0.1	27	change SD034200280(20K ohm) to SD034200180(2K ohm)	2009.8.24	EVT
12	Change PR90	Modify power sequence	0.1	27	change SD034100280(10K ohm) to SD034100180 (1K ohm)	2009.8.24	EVT
13	Change PC77 & PC86 & PC96	Modify power sequence	0.1	27	Change PC77 & PC86 & PC96 to pop change SE076104KM8(0.1uf) to SE000000K80 (1uf)	2009.8.24	EVT
14	Change PC109	Change part number	0.1	27	change SE076104KM8(0.1uf) to SE076104K80(0.1uf)	2009.8.24	EVT
15	Change PL3.PL4	To slove high frequency noise	0.1	26	change SH00000BU00(4.7uH) to SH00000BS00(8.2uH)	2009.8.27	EVT
16	Change PL9	For design change	0.1	29	change SM01000BY00 to SM01000C000	2009.9.4	DVT
17	Change PL4	To improve +5VALWP efficiency	0.1	26	change SH00000BS00(8.2uH) to SH00000F900(4.7uH)	2009.9.10	DVT
18	Change PR209	Modify CPU CORE OCP	0.1	29	change SD028180180(1.8K ohm) to SD034237180 (2.37K ohm)	2009.9.30	PVT
19							
20							
21							
22							
23							

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<2009/4/28>
Update new power schematic,
release first version NAV50 schematic

<2009/04/29>
Add R1182 R1183 L3 on page 9
Change J3 to R1184 on page 13

<2009/04/30>
Change JDIM1 to SP07F001720 on page 7
Del SATA1 Port on page 12
Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
Add CRT_DET# on page 10
Add CRT_DET# circuit on page 13
Add 3 LEDS on page 16
Add BT/BTN Board CONN. on page 16
Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
Add INVT_PWM on Page 5
Del R323 on page 5
C74 change to 2.2U_0603 on page 6
C267 change to 22U on page 6
C391 change to 0.1U on page 6
Del C67 C35 C33 C36 on page 6
Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
Follow Intel checklist, add R52 on FSB on page 8
Add D5 D7 D8 on page 4
Add R174 on page 9
Add PCI_RST# on page 11
Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
Modify SRC CLK PORT LIST on page 8
Del CLKREQ_LAN# on page 8
Change PCIE Port list on page 13
Change USB Port list on page 13
Add W/L 3G SW on page 16
Del R103 on page 18

<2009/05/13>
Change JMINI1 to PCIE Port 3 on page 15

<2009/05/14>
Page8 Change C174 C175 to 10U_0603

<2009/05/14>
Update New Power schematic
Del R376 R377 on page 8
Del D5 D7 D8 on page 4
Change JLVDS1 to SP010006810 on page 9
Add D6 for EMI on page 9
Change C1106 to C_0603 type on page 9
Change USB_OC# on page 13
Add USB Port2 on page 20
Change JP11 Pin define & Add D22 on page 19
Change C512 to 1u_0402 on page 15
Add U29 (MEDIA_LED#) on page 16

<2009/05/19>
Update new clock GEN co-lay schematic on page 8

<2009/06/05>
Update new clock GEN co-lay schematic on page 8
Follow Intel check list change C161 C165 to 27P on page 8
Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
Update New Power schematic 06/06 version
Page 13- a. Del R203 (pull-up GPIO6 Resister)
b. Change R1184 NU
Page 17- a. Add VGATE
b. Del R1294
c. Change D30 NU
d. Change R1295 to 0 ohm
e. Add R1309 0 ohm on EC_RSMRST#
f. Pull-up LAN_WAKE# +3VALW
g. ICH_POK change to PCH_POK
h. Pull-up KB_RST# to +3VS
Page 10- a. Add R1283 R1284 , Change R247 R249 to 10 ohm
b. Add @ on U10 U11 C301 C298
c. Del C302 C300 R1281 R1287

<2009/06/10>
Page 7- Add C116 @
Page 22- Modify USB_OC#1_2 to USB_OC#2
Page 17- Modify PLTRST# to PCI_RST#
Page 17- Add @ on R1311

<2009/06/12>
Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
Page8 Add C1145 C1146 C1147
Page10 Move CRT_DET# from Page13 to Page10
Page13 Add +RTCVCC circuit

<2009/06/15>
Update New Power schematic (change PBJ1 to PJP3)
Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
Page7 Modify DDR Command Control Pin pull-high Resister location
Page9 Change R577 to 0402 type

<2009/06/17>
Update New Power schematic 06/17
Page9 modify LVDS Conn. Pin define
Page9 Del C1110
Page4 Add EMI solution D38 D39 D40

<2009/06/18>
Update New Power schematic 06/18
Page8 modify U4 Pin define and Q31
Page13 Add R1376, R1377
Page15 Modify C403
Page23 Modify H11

<2009/06/19>
Page4 Add new signal CPU_ITP , CPU_ITP#
Page5 ADD R1378
Page6 ADD C1152, C1153, C1154 C1160, C1161, C1162
Page7 DDR_A_D8與DDR_A_D9互換
Page8 ADD R1379, R1380, U77, R1381, C1157, R1382, R1383, R1384, C1157
Page8 DEL C390
Page9 ADD C1156
Page11 DEL R1322, R1154
Page13 DEL U77, ADD C1158
Page17 ADD C1159

<2009/06/22>
Page22 change IO Conn. pin34 from 48M to USB_ON#
Page10 change JCR11 P/N to SP010906182

<2009/06/23>
Page15 Add C1163 C1164 C1165 C1166
Page18 change PWR/B Conn. P/N to SP01000H300
Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
Page8 Change C1350 C1351 to 0402 type
Page10 Add R1385 R1386 on JVG_A_HS JVG_A_VS

<2009/06/25>
Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B

<2009/06/29>
Page16 Change JP24 to ACES_88266_05001
Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
Page18 Change PWR_LED# to PWR_PWM_LED#
Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
Update New Power schematic 07/02
Page9 Add C1167 C1168 for RF request.
Page13 Change R223 to 100K
Page16 change JP24 to ACES_85201-0505N
Page17 Del R1387 R1388 on EC Pin97
Page17 Add New Board ID to separate NAV50 NAV60
Page17 Change 展頻IC to SA00003J400 (New)
Page18 Add D41 for ESD

<2009/07/03>
Page18 Add D41.2 to PWR_PWM_LED#
Page8 Change co-lay net name to +1.5VM_CK505
Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
Page18 Add pwr switch for NAV50

<2009/07/08>
Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
Page9 Change JLVDS1 to P/N ACES_88341-3001 30P
Page17 del PM_1.8V(U6.82) , Del R1310 R1311
Page18 Del D41

<2009/09/03>
Page7 Change C112 to 0402 type
Page8 Add T6 on CLK_48M_CR
Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
Page21 Del H12

<2009/09/08>
Update Power schematic 0904
Page18 Change R1388 to 100 ohm 0402
Page18 Change LED1 to SC591NB5A00

<2009/09/10>
Update Power schematic 0910
Page22 unmount Q6 Q8

<2009/10/07>
Page4 U71 Change to SA00003M800
Page6 R26 Change to SHI00009C00
Page13 R152 Change to SD034200A80
Page18 R1388 Change to SD028510A80

<2010/04/29>
update new bom

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